CLAIMS

1. A system for designing an integrated circuit (IC) comprising:

a circuit comprising (i) a functional portion and (ii) a logic portion connected to said functional portion and configured to detect, fix or verify fixes of errors in said function portion.

2. The system according to claim 1, wherein said logic portion includes one or more interfaces, and said system further comprises:

a debugging/bug fix circuit configured to detect errors in said logic portion through said one or more interfaces.

3. The system according to claim 1, wherein said system comprises a diagnostic architecture using an FPGA core in a system on a chip design.

4. The system according to claim 2, wherein said system is further configured to (i) provide ease in bringing up, (ii) verification and (iii) debugging, each by interconnecting said circuit and said debugging/bug fix circuit.

5. The system according to claim 1, wherein said system is further configured to provide one or more programming options of said circuit.

6. The system according to claim 2, wherein said system is further configured to allow observation of one or more signals by said debugging/bug fix circuit.

7. The system according to claim 6, wherein said system is further configured to allow observation of said one or more signals when running in a normal mode.

8. The system according to claim 1, wherein said system is further configured to run in a single step mode.

9. The system according to claim 8, wherein said system is further configured to run in said single step mode when controlled by a gate or a core.

10. The system according to claim 9, wherein said core comprises said FPGA core.

11. The system according to claim 9, wherein said core is programmable.

12. The system according to claim 2, wherein said debugging/bug fix circuit comprises a debugging workstation.

13. The system according to claim 2, wherein said debugging/bug fix circuit is further configured to allow one or more debugging features.

14. The system according to claim 13, wherein said one or more debugging features support triggering and tracing based on one or more internal signals.

15. The system according to claim 13, wherein said one or more debugging features support dynamically changing host register values.

16. The system according to claim 13, wherein said one or more debugging features provide complex monitoring functions.

17. The system according to claim 1, wherein said system is further configured to reduce debugging/verification time and/or improve product time to market.

18. The system according to claim 1, wherein said circuit is further configured to operate in a normal mode and a single step mode.

19. The system according to claim 18, wherein said normal mode is configured to allow said circuit to present one or more internal signals of said functional portion and said single step mode is configured to provide a plurality of signals of said functional portion.

20. The system according to claim 18, wherein a scan chain is used to diagnose or fix a bug via the logic portion.

21. The system according to claim 18, wherein the programmable portion is further configured to bridge one or more of said plurality of signals between a plurality of modules.

22. The system according to claim 2, wherein said debugging/bug fix circuit and said circuit are configured to generate one or more debugging features.

23. The system according to claim 2, wherein said debugging/bug fix circuit is configured to work with Computer Aided Design (CAD) software to provide one or more diagnostic functions.

24. The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of searching for a specific signal pattern, tracing the internal state machine, triggering on a programmed condition and other appropriate diagnostic functions.

25. The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of on the fly monitoring of a correctness of a bus protocol, and implementing statistics counting to measure the performance and the testing coverage.

26. A method for diagnostics comprising the steps of:

(A) interfacing a chip with a core;

(B) presenting one or more internal signals of said chip; and

(C) verifying or fixing bugs in said chip with said one or more internal signals.

27. A computer readable medium configured to store instructions for executing the steps of claim 26.

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